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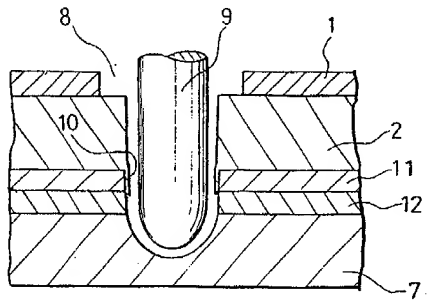
(54) Method for dividing a semiconductor wafer comprising a semiconductor layer and a metal layer into chips.

(57) According to a method for producing a semiconductor device, a metal layer serving as a heat sink is formed over the rear surface of a semiconductor wafer, dicing lines, along which the metal layer is divided into chips, are formed by partially etching the semiconductor wafer, a layer comprising a material having higher hardness than that of the metal layer is put on the rear surface of the metal layer via an adhesive agent, a dicing tape is put on the rear surface of the layer having high hardness, the metal layer is diced along the dicing lines, resulting in a plurality of semiconductor chips for diebonding. Therefore, a burr on the rear surface of the metal layer owing to ductility of the metal layer can be reduced. In addition, since the dicing tape is used, a rapid transition to the subsequent process is possible.

FIG. 3

(b)



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FIELD OF THE INVENTION

The present invention relates to a method for producing a semiconductor device and, more particularly, to an improvement of processing precision and working efficiency in dicing process.

BACKGROUND OF THE INVENTION

Figure 4 is a perspective view showing a structure of a semiconductor device which is produced by a prior art method. In figure 4, reference numeral 1 designates a semiconductor substrate. An IC pattern 6 is produced on the surface of the substrate 1. A metal layer 13, which serves as both of a grounding electrode and a heat sink, is provided on the rear surface of the substrate 1. The metal layer 13 is connected with the surface of the substrate 1 through via-holes 5.

Figure 5 is a diagram showing a prior art method for dividing a semiconductor wafer into chips. In figure 5, an elastic dicing tape 7 is attached to the rear surface of the metal layer 13. This elastic dicing tape 7 makes processes to be carried out after the dividing process easy ones. Dicing lines 8 are formed by removing portions of the semiconductor substrate 1 using chemical etching. Reference numeral 9 designates a dicing blade and numeral 10 designates a burr.

A wafer comprising the semiconductor substrate 1 and the metal layer 13 is put on the elastic dicing tape 7 and then it is divided into chips along the dicing lines 8 using the dicing blade 9. The metal layer 13 of a chip which is produced in this way has smooth side surfaces.

In the above-described method for producing a semiconductor device, owing to ductility of the metal layer 13 during the dicing, a burr 10 is generated along the shape of the dicing blade 9 which is inserted toward the dicing tape 7 attached on the rear surface of the metal layer 13. This burr 10 causes an insufficient junction when the chip is diebonded on a die pad in a later process.

For example, when a semiconductor wafer comprising a GaAs semiconductor substrate of 30 microns thickness and an Au layer of 50 microns thickness is diced, a burr of approximately 20 to 30 microns is generated on the rear surface of the Au layer.

Another method for dividing the wafer into chips is conducted by etching using a mask as shown in figure 6. More specifically, resist films 14 serving as etching mask are formed on the semiconductor substrate 1 except for regions 8' corresponding to the dicing lines 8 shown in figure 5 and then the wafer is soaked into an etchant. In this method, although no burr is generated on the rear surface of the chip, it is difficult to control the dimension of the side surfaces of the chip. In addition, the chips thus produced using etching are separated from each other, resulting in incapability of a rapid transition to the subsequent diebonding process. This results in a poor production yield.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide a method for producing a semiconductor device, by which production yield is improved and a sufficient junction can be achieved at diebonding.

Other objects and advantages of the present invention will become apparent from the detailed description given hereinafter; it should be understood, however, that the detailed description and specific embodiment are given by way of illustration only, since various changes and modifications within the spirit and the scope of the invention will become apparent to those skilled in the art from this detailed description.

According to an aspect of the present invention, when a wafer comprising a semiconductor layer and a metal layer is divided into chips, a layer comprising a material having higher hardness than that of the metal layer is put on the rear surface of the metal layer via an adhesive agent, a dicing tape is attached to the rear surface of the layer having high hardness, and the wafer is divided into chips along dicing lines on the semiconductor layer using a dicing blade. Therefore, a burr on the rear surface of the metal layer owing to ductility of the metal layer is reduced. In addition, since the dicing tape is used, a rapid transition to the subsequent process is possible.

According to another aspect of the present invention, the material having higher hardness than that of the metal layer has a light transmitting property and the adhesive agent decreases its adhesion when exposed to light. Therefore, the chip can be easily removed from these materials.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a perspective view of a semiconductor device which is produced by a production method in accordance with an embodiment of the present invention;

Figure 2 is a cross-sectional view of the semiconductor device of figure 1;

Figures 3(a) is a cross-sectional view of a semiconductor wafer in a dicing process in accordance with an embodiment of the present invention and figure 3(b) is an enlarged view of a portion of the wafer;

Figure 4 is a perspective view of a semiconductor device which is produced by the prior art production method; Figure 5 is a cross-sectional

view of a semiconductor wafer in a dicing process in accordance with the prior art; and
Figure 6 is a cross-sectional view of a semiconductor wafer in a dicing process using etching in accordance with the prior art.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

An embodiment of the present invention will be described in detail with reference to the drawings.

Figure 1 is a perspective view of a semiconductor chip produced by a production method in accordance with an embodiment of the present invention, viewed from its bottom surface, and figure 2 is a cross-sectional view thereof. In these figures, reference numeral 1 designates a semiconductor substrate on which an IC pattern is formed. A gilded layer 2 is connected with the IC pattern on the substrate 1 through via-holes. This gilded layer 2 serves as both of a grounding electrode and a heat sink.

In this structure, the burr of the gilded layer 2 protruding from the rear surface 3 at the side surface 4 is below 5 microns. In addition, the side surface 4 of the gilded layer 2 is produced smooth due to the dicing.

Figure 3(a) is a cross-sectional view of a semiconductor wafer in a dicing process in accordance with an embodiment of the present invention, and figure 3(b) is an enlarged view of a portion of the wafer. In these figures, the same reference numerals as those of figures 1 and 2 designate the same or corresponding parts. A sapphire wafer 12 of 150 to 200 microns thickness is attached to the rear surface of the gilded layer 2 using an adhesive agent 11 of 5 microns or less thickness so as to suppress the generation of burr due to ductility of the gilded layer 2 at the time of dicing. A dicing tape 7 is attached to the rear surface of the sapphire wafer 12. Reference numeral 9 designates a dicing blade. In addition, the adhesive agent 11 decreases its adhesion when exposed to light.

Similarly as in the prior art, the gilded layer 2 is divided into chips along the dicing lines 8, which are formed by removing portions of the substrate 1 by chemical etching, with the dicing blade 9. In this dicing process, the burr 10 due to the ductility of the gilded layer 2 is reduced to 5 microns or less, which is equal to the thickness of the adhesive agent 11, because the sapphire wafer 12 having higher hardness than that of the gilded layer 2 is provided beneath the gilded layer 2 via the adhesive agent 11.

Next, each semiconductor chip thus separated is removed from the dicing tape 7. Thereafter, light is irradiated on the semi-transparent sapphire wafer 12 at the rear surface of the chip to reduce the adhesion of the adhesive agent 11, whereby the sapphire wafer 12 is easily removed from the gilded layer 2.

In the above-described embodiment, the sapphire wafer 12 having higher hardness than that of the gilded layer 2 is put on the rear surface of the gilded layer 2 having large ductility via the adhesive agent 11, the dicing tape 7 is attached to the rear surface of the sapphire wafer 12, and then the gilded layer 2 is diced. Therefore, the burr to be generated on the rear surface of the gilded layer 2 is suppressed to about 5 microns, which is equal to the thickness of the adhesive agent 11. The burr of about 5 microns exerts no influence on the subsequent diebonding process and a sufficient junction can be achieved.

In addition, since the dicing is carried out using the dicing tape 7, it is possible that the dicing process rapidly transits to the subsequent diebonding process, resulting in an improved production yield.

Since the sapphire wafer 12 has a light transmitting property and the adhesive agent 11 decreases its adhesion when exposed to light, the sapphire wafer 12 can be easily removed from the chip by irradiating light on the sapphire wafer 12.

Furthermore, since the division of wafer into chips is performed by dicing using the dicing blade 9, the cutting plane (side surface of gilded layer 2 of each chip) is produced smooth, so that the chip size is easily controlled as compared with the case where it is performed by etching.

While in the above-described embodiment sapphire is used as a material having higher hardness than that of the metal layer 2, any other material, such as glass, may be used so long as it is harder than the metal layer 2. Also in this case, the same effect as described above can be obtained.

While in the above-described embodiment the gilded layer is used as the metal layer 2 formed on the rear surface of the semiconductor substrate 1, the same effects as described above can be obtained even when other metal layers having ductility, such as silver or copper, are used.

While in the above-described embodiment the adhesive agent 11 has a property of decreasing its adhesion when exposed to light, other adhesive agents may be used so long as the semiconductor chip is easily removed.

While in the above-described embodiment the thickness of the adhesive layer 11 is below 5 microns, it is not limited thereto. The adhesive layer may be thicker than 5 microns so long as the burr of the metal layer 2 does not affect the diebonding process.

As is evident from the foregoing description, according to the present invention, when a wafer comprising a semiconductor layer and a metal lay-

er is divided into chips, a layer comprising a material having higher hardness than that of the metal layer is put on the rear surface of the metal layer via an adhesive agent, a dicing tape is attached to the rear surface of the layer having higher hardness, and the wafer is diced along dicing lines using a dicing blade. Therefore, the burr of the metal layer at the dicing can be reduced and a sufficient junction can be achieved in the subsequent diebonding process. In addition, since the dicing tape is used, the production yield can be improved.

Furthermore, since the layer having higher hardness has a light transmitting property and the adhesive agent decreases its adhesion when exposed to light, the chip can be easily removed from that layer by irradiating light on that layer, resulting in high work efficiency.

Claims

1. A method for producing a semiconductor device comprising process steps of:

   forming a metal layer serving as a heat sink over the rear surface of a semiconductor wafer;

   forming dicing lines, along which said metal layer is divided into chips, by etching said semiconductor wafer;

   putting a layer comprising a material having higher hardness than that of said metal layer on the rear surface of said metal layer via an adhesive agent;

   putting a dicing tape on the rear surface of said layer having higher hardness; and

   dicing said metal layer along said dicing lines, resulting in a plurality of semiconductor chips for diebonding.

2. A method for producing a semiconductor device in accordance with claim 1 wherein said material having higher hardness than said metal layer has a light transmitting property and said adhesive agent decreases its adhesion when exposed to light.

3. A method for producing a semiconductor device in accordance with claim 2 wherein said material harder than said metal layer is sapphire.

4. A method for producing a semiconductor device in accordance with claim 2 wherein said material harder than said metal layer is glass.

FIG. 1

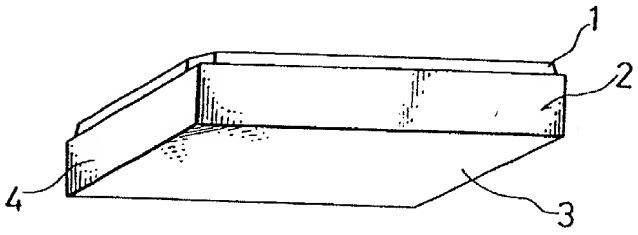


FIG. 2

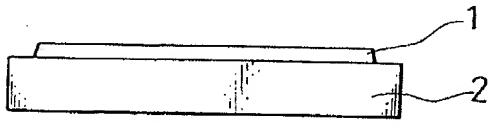
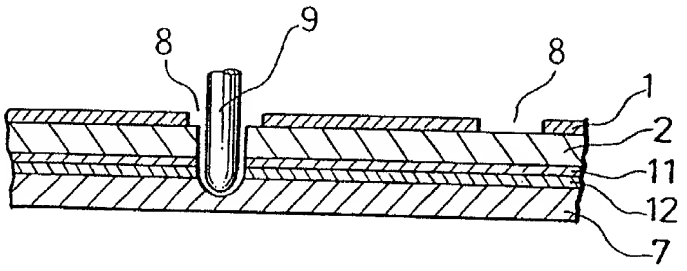


FIG. 3

(a)



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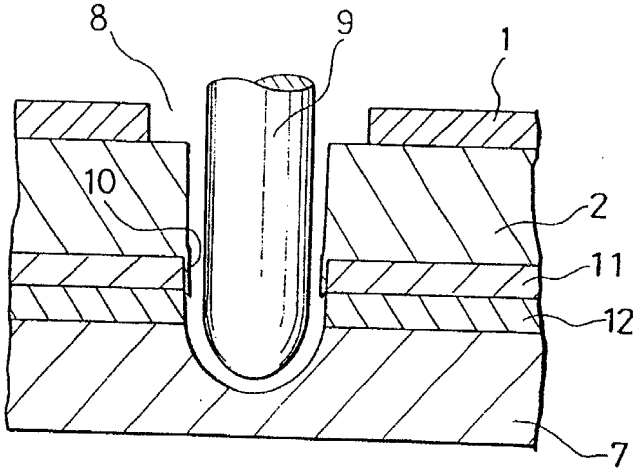

FIG. 4 (PRIOR ART)

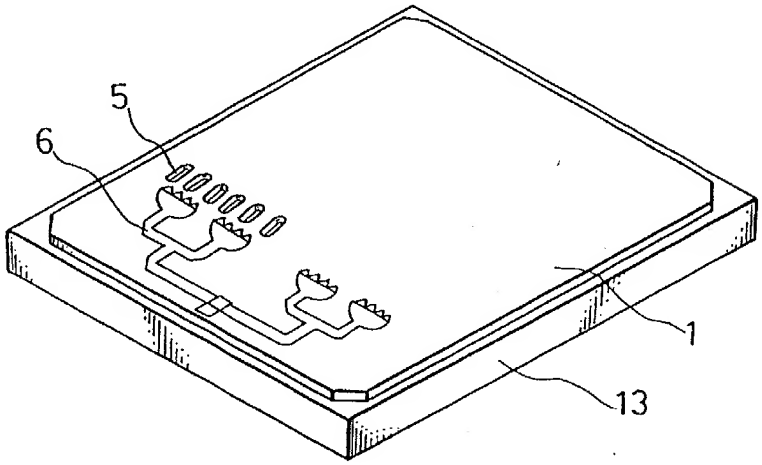

FIG. 5 (PRIOR ART)

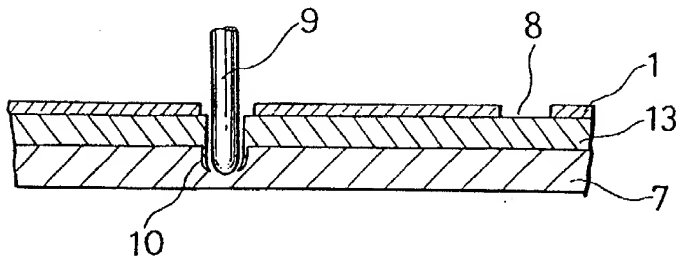

FIG. 6 (PRIOR ART)